First Proposal for Production Module Testing

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Analyze module production sequence

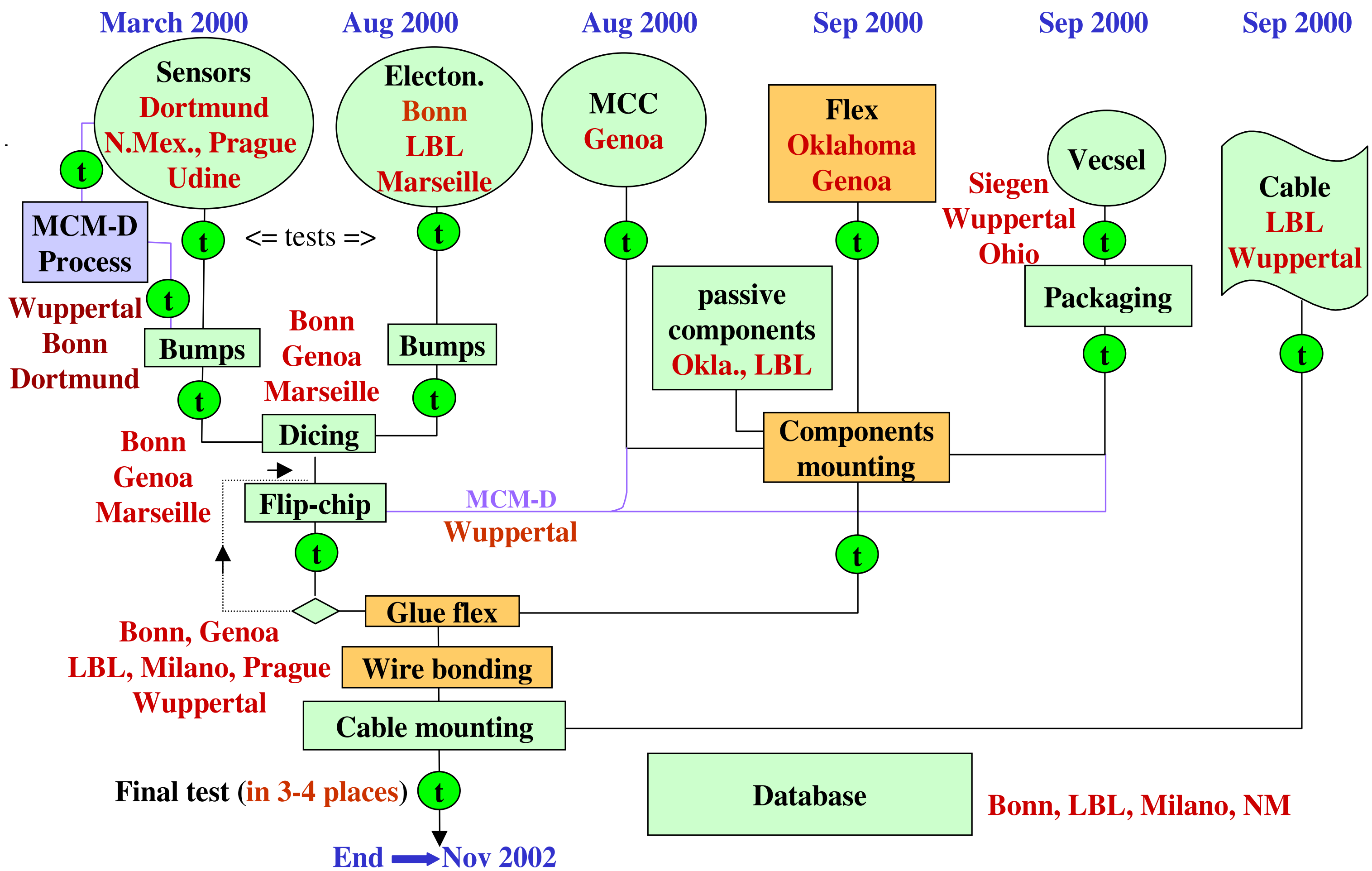
- Address what electronics (and sensor) testing needs exist at each step

What are the corresponding needs for test hardware ?

- PLL-like system for basic FE + MCC testing
- MCC tester for dedicated MCC evaluation
- New PLL+PICT for real parametric testing of FE chips and MCC interface
- Extension of PCC for burn-in testing

Overview of Module Assembly Flow

Figure presented for LHCC (from Giovanni/Pierre):



- There are many "testing" entries inserted in this flow. I believe some of these will be "inspection" and some may not exist (parts will not leave vendors).
- Major uncertainy is whether optolink mounts on Flex or on cable harness.

Basic Testing Points in Module Assembly

Initial testing of components:

- Wafer probing of FE, MCC, and sensors
- Proposals for hardware and procedures exist and will need to be refined by those communities in the pixel effort.
- Continuity testing of Flex, and initial testing of optolink (if optolink is on Flex).
- No proposal yet made for how optolinks will initially be evaluated.
- One issue is what kind of periodic irradiation testing is required? Periodically dice single chips from both sensor and electronics wafers, irradiate and characterize ? Periodically build modest number of single-chip assemblies and test ?

Followed by:

- Bumping, Thinning, Dicing, Flipping steps
- Personally believe that insertion of actual testing steps (as opposed to inspection of various kinds, including X-ray bump inspection) in this sequence is likely to lower yield and significantly increase time and manpower.
- This will depend on our experience with real production volumes (example: CDF SVX3 chips suffered additional 10% yield loss after dicing, which is not understood and presently requires re-probing of all electronics die at single-die level in order to achieve acceptable re-work levels in module assembly)

Next major test point is for multi-chip modules:

- Have set up prototype system at LBL for this, including a special vacuum chuck with alignment ledges on two sides, 4 vacuum holes under each of 16 FE chips, and adjustable HV bias contact for sensor plus deep-access single-chip probe card. This should allow us, when using a p-spray sensor and a dark-box, to carry out complete digital and analog module testing. This could include source tests to check bump-bonding connectivity before more resources are invested in module.
- Have probed one IZM module and one Alenia module.
- IZM module could not be probed with our standard Be-Cu needle probe card due to problem of bond-pad contamination. This is a well-known problem already at the wire-bonding stage, and arises because of under-bump-metal deposition on wire-bond pads followed by wet-etch which does not remove all metal. Visual inspection of pads shows clear contamination (smooth Al pad replaced by grainy, crystalline appearance). Wire-bonding with Al wire with elevated bond parameters normally works. Probing seemed to be impossible without resorting to much harder needles which could easily damage the wire-bond pads.
- Alenia module could be probed digitally (register tests and digital hit injection). Analog performance was extremely poor (essentially no threshold observed). This could be the usual “FE-B chips and Alenia bumps” problem (but noise was worse than for single chips), or it could be noise problems in the test setup or both.

- Further work required with higher quality modules (IZM modules processed with wire-bond pads masked during metalization, Alenia modules flipped with new electronics which should improve noise performance).

Assembly procedure for Flex:

- All tested components are mounted on Flex. MCC is either wire-bonded and encapsulated, or more exotic attachment methods could be used to reduce height (TAB or bump-bonding with some encapsulation to prevent delamination from Flex). Rework probably not useful at this level.
- Complete Flex is tested. A simple set of capacitance and continuity measurements would test the power distribution. Real electrical testing would require special probe card(s) and something like the MCC tester being built by Genova, since one needs to supply fake FE data to one or more of the MCC input FIFOs from the FE wire-bond pads, and check resulting outputs. Will MCC testing be available at production sites ?
- More development work in this area is needed, otherwise we will continue losing modules due to bad/defective components.

Next step is assembly of Flex and multi-chip module:

- After this is completed, test cycle would be done using a PLL-like system. This should involve placing the module in a vacuum chuck and Nitrogen box, which would be temperature cycled in an environmental chamber. Perhaps one would do an initial test at the minimum allowed operating temperature (-20 C ?), followed by a series of temperature cycles up and back down, with further testing, to check for poor connections or mechanical problems.
- This would be followed by a burn-in sequence, in which perhaps 20 modules would be processed in parallel (module production rate per site at least 2 modules per day, burn-in of perhaps 10 days). The modules could be operated by a PLL-like system with an input/output multiplexer so that all would receive XCK, L1, etc., but one would periodically cycle through all of them running standard module tests.
- It is not clear whether this burn-in test should involve elevated stress levels (e.g., higher T) in order to provoke failures of weak modules, or whether this would simply harm otherwise good modules. Whatever temperature cycling is involved must be included in the initial mechanical analysis to be sure it does no mechanical damage.

Tests to be done after single module burn-in could include:

- Standard wafer-probe tests (register tests, digital inject pattern tests, analog threshold scans)
- Additional charge calibration as done now for H8 (cross-correlates internal charge injection with narrow X-ray source like Cd109)
- Additional timing scans to check timing uniformity on module and timewalk performance. Possibly use laser scan to provide absolute external time check, in which case there should be at least several windows in the Flex for laser access.
- Issue: Flex obscures easy access to sensor surface, making laser and low-E X-ray source scans rather painful. X-ray source like Cd109 very effective for checking module (self-trigger rate of 50KHz achieved allowing rapid test). Higher energy X-ray (Am241) has much lower counting rate. Switching to β source (Sr or Ru) requires collimation and trigger for high-quality test, which is slow.

Following these tests, modules would be placed on mechanical structures (sectors and staves):

- Would again perform basic module characterizations, this time with cooling. Presumably would check thermal performance with IR imaging system. This could probably still be performed with PLL-like system, one module at a time.
- As local mechanical structures get assembled into global structure, and real cable harnessing is connected, would continue to perform frequent basic checks. However, as the number of modules continues to increase, will need to progress to real ROD-based readout system with real optical readout.

Questions and Issues:

Test Electronics needs:

- For wafer probing of FE chips, an upgraded “pixel IC tester” has been proposed, including an upgraded PLL and a new PCC-like card called PICT. A wafer probe site may have to probe as many as 1K wafers or 100K die. This leads to a goal of 1 minute per die for test, or about 2 hours per wafer (could then complete testing in one year).
- For wafer probing of MCC chips, expect to perform testing commercially with digital IC tester. Note that testing at increased XCK will be needed to measure the performance margins and make sure the chips will work after irradiation.
- Routine module testing can be handled by a PLL-like system. Question: can it be the present PLL, or are upgrades required ? Goal would be fairly complete module characterization in 1 hour. Some issues:
  - On-board SRAM for single-chip versus module histogramming (large speed gain possible)
  - New FPGA to improve programmability (little room left now for adding functionality)
  - Operation and testing at elevated XCK or CCK frequencies
- For any serious testing of MCC, need a dedicated system capable of supplying programmable data to up to 16 FE inputs. Although PLL could be programmed to use MCC receiver mode for some of these tests, the data should really be injected through the correct pads on the Flex or MCM-D.

- For the module burn-in phase, a PCC-like card with multiplexed connections to many modules should work quite well. Cycling the PLL single-module test capability through each of the modules under burn-in should give adequate operation (i.e. ROD-like multi-module handling should not be necessary).

Schedule:

- PLL-like tester and parametric testing being designed and built at LBL, and should be ready by Spring 00 to allow complete FE-D/FE-H evaluation.
- MCC test capability being developed by Genova. Some thought should be given to its use during production module assembly.
- Final production burn-in system could wait until early 2001, and should not be very complex to engineer.

Connection issues:

- Module has two basic connections: power and data/control. The first is a low-mass Flex tape, the second is either optical onto the module or optical on the harness and electrical onto the module. These connections will have to be temporarily connected/disconnected during various stages of testing without any risk to the module itself.
- Geometry is not yet clear. With there be extension tabs ? Will there be end or side attachment (disks and staves different ?). Stress relief is important as Flex can easily peel off module, and wire-bonds can easily be damaged.
- For power connection: how can we reliably make/break up to 1A power connections to Flex without any “aging” effect or stress induced in Flex ? Flex has an extension which can fit into a standard Flex connector (testing only)? Clamp connection integrated into vacuum support fixtures ?
- For optical-on-module: how can we reliably make/break this connection ? GEC lids do not provide adequate solution, and presently forsee first MT connector at 5 meters from module. Hence, in this case would use MT connector but carry around 5m of fiber “pigtail” with the module (dangerous).
- For optical-on-harness: need additional electrical connection to module, which could be made in the same way as the power connections ?
- Some prototyping of these connections is needed !